This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor field-effect transistor device comprising:

a first strained layer of semiconductor material doped of a first dopant type ~~formed~~ located on a substrate;

a source region and a drain region implanted with dopants of a second opposite type located at least within said first strained layer;

a gate electrode separated from the first strained layer by a dielectric region, and positioned between said source and drain regions;

said substrate having one or more threading dislocations, misfit dislocations or crystal defects that extend continuously from the source region to the drain region at an interface between said first strained layer of semiconductor material and said substrate, and

a peak concentration of blocking impurity dopant materials selected from the group consisting of ~~comprising:~~ In, Pb, Sb and Sn~~, that partially or fully occupies each said one or more threading dislocations, misfit dislocations or crystal defects along~~ located substantially at said interface, wherein said blocking impurity dopant materials partially or fully occupy each of said one or more threading dislocations, misfit dislocations or crystal defects at said interface and substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along said interface.

2. (Currently Amended) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said first strained layer of semiconductor material comprises a material selected from the group ~~comprising~~ consisting of: Si, SiGe, SiGeC, [[or]] and Ge.

3. (Cancelled)

4. (Previously Presented) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said substrate comprises a SiGe relaxed substrate.

5. (Original) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said source and drain dopants of said second type comprise P, As or Sb, singly or in combination thereof, and said blocking impurity is In.

6. (Original) The semiconductor field-effect transistor device as claimed in Claim 1, wherein said source and drain dopants of said second type comprise B or In, singly or in combination thereof, and said blocking impurity is Sb.

7. (Currently Amended) The semiconductor field-effect transistor device as claimed in Claim [[1]] 22, wherein said blocking impurity is a neutral-type impurity.

8. (Currently Amended) The semiconductor field-effect transistor device as claimed in Claim [[7]] 22, wherein said blocking impurity is a group IV impurity.

9. (Currently Amended) The semiconductor field-effect transistor device as claimed in Claim [[1]] 22, wherein said blocking impurity dopant comprises C, singly or in combination with said Sn or Pb.

10-21. (Cancelled)

22. (New) A semiconductor field-effect transistor device comprising:

a first strained layer of semiconductor material doped of a first dopant type located on a substrate;

a source region and a drain region implanted with dopants of a second opposite type located at least within said first strained layer;

a gate electrode separated from the first strained layer by a dielectric region, and positioned between said source and drain regions;

said substrate having one or more threading dislocations, misfit dislocations or crystal defects that extend continuously from the source region to the drain region at an interface between said first strained layer of semiconductor material and said substrate, and

a peak concentration of blocking impurity dopant materials located substantially at said interface, wherein said blocking impurity dopant materials partially or fully occupy each of said one or more threading dislocations, misfit dislocations or crystal defects at said interface and substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along said interface.

23. (New) A semiconductor field-effect transistor device comprising:

a first strained layer of semiconductor material doped of a first dopant type located on a substrate;

a source region and a drain region implanted with dopants of a second opposite type located at least within said first strained layer;

a gate electrode separated from the first strained layer by a dielectric region, and positioned between said source and drain regions;

said substrate having one or more threading dislocations, misfit dislocations or crystal defects that extend continuously from the source region to the drain region at an interface between said first strained layer of semiconductor material and said substrate, and

a peak concentration of blocking impurity dopant materials having a concentration between 10^{17} cm^{-3} to 10^{19} cm^{-3} located substantially at said interface, wherein said blocking impurity dopant materials partially or fully occupy each of said one or more threading dislocations, misfit dislocations or crystal defects at said interface and substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said threading dislocations, misfit dislocations or crystal defect along said interface.